WHAT IS CLAIMED IS:

1. A method of manufacturing a vertical MOS transistor, comprising:

carrying out anisotropic etching for a region in which a trench is intended to be formed on a main surface of a semiconductor substrate of a first conductivity type to form the trench;

forming a gate oxide film over the main surface of the semiconductor substrate of the first conductivity type and along wall surfaces of the trench;

depositing a polycrystalline silicon layer so as to overlie the gate oxide film;

etching the polycrystalline silicon layer so as to remove the polycrystalline silicon layer overlying the main surface of the semiconductor substrate and so as to remove the polycrystalline layer within the trench to a predetermined depth from the main surface of the semiconductor substrate to form a gate electrode within the trench;

implanting an impurity of a second conductivity type into the main surface of the semiconductor substrate of the first conductivity type and thermally diffusing the impurity of the second conductivity type to form a body region of the second conductivity type;

implanting an impurity of the first conductivity type into the main surface of the semiconductor substrate to form a source

region of the first conductivity type;

implanting an impurity of the second conductivity type into the main surface of the semiconductor substrate to form a body contact region of the second conductivity type;

depositing an intermediate insulating film over the main surface of the semiconductor substrate and the gate electrode;

etching back the intermediate insulating film overlying the main surface of the semiconductor substrate so as to entirely expose the source region and the body contact region constituting the main surface of the semiconductor substrate; and

forming a source metal electrode over the main surface of the semiconductor substrate.

2. A method of manufacturing a vertical MOS transistor, comprising:

carrying out anisotropic etching for a region in which a trench is intended to be formed on a main surface of a semiconductor substrate of a first conductivity type to form the trench;

forming a gate oxide film over the main surface of the semiconductor substrate of the first conductivity type and along wall surfaces of the trench;

depositing a polycrystalline silicon layer so as to overlie the gate oxide film;

etching the polycrystalline silicon layer so as to remove the

polycrystalline silicon layer overlying the main surface of the semiconductor substrate and so as to remove the polycrystalline layer within the trench to a predetermined depth from the main surface of the semiconductor substrate to form a gate electrode within the trench;

implanting an impurity of a second conductivity type into the main surface of the semiconductor substrate of the first conductivity type and thermally diffusing the impurity of the second conductivity type to form a body region of the second conductivity type;

implanting an impurity of the first conductivity type into the main surface of the semiconductor substrate to form a source region of the first conductivity type;

implanting an impurity of the second conductivity type into the main surface of the semiconductor substrate to form a body contact region of the second conductivity type;

depositing a first insulating film over the main surface of the semiconductor substrate;

removing the first insulating film overlying the main surface of the semiconductor substrate by utilizing the anisotropic etching to form side spacers made of the first insulating film on the wall surfaces of the trench overlying the gate electrode;

depositing an intermediate insulating film over the main surface of the semiconductor substrate and the gate electrode;

etching back the intermediate insulating film overlying the main surface of the semiconductor substrate so as to entirely expose the source region and the body contact region constituting the main surface of the semiconductor substrate; and

forming a source metal electrode over the main surface of the semiconductor substrate.

3. A method of manufacturing a vertical MOS transistor, comprising:

carrying out anisotropic etching for a region in which a trench is intended to be formed on a main surface of a semiconductor substrate of a first conductivity type to form the trench;

forming a gate oxide film over the main surface of the semiconductor substrate of the first conductivity type and along wall surfaces of the trench;

depositing a polycrystalline silicon layer so as to overlie the gate oxide film;

etching the polycrystalline silicon layer so as to remove the polycrystalline silicon layer overlying the main surface of the semiconductor substrate and so as to remove the polycrystalline layer within the trench to a predetermined depth from the main surface of the semiconductor substrate to form a gate electrode within the trench;

implanting an impurity of a second conductivity type into the

main surface of the semiconductor substrate of the first conductivity type and thermally diffusing the impurity of the second conductivity type to form a body region of the second conductivity type;

implanting an impurity of the first conductivity type into the main surface of the semiconductor substrate to form a source region of the first conductivity type;

implanting an impurity of the second conductivity type into the main surface of the semiconductor substrate to form a body contact region of the second conductivity type;

depositing a first insulating film in a thickness in which the trench is perfectly filled with the first insulating film and the surface of the first insulating film reaches the main surface of the semiconductor substrate to perfectly flatten a surface of the first insulating film overlying the main surface of the semiconductor substrate;

etching back the first insulating film so as to remove the first insulating film overlying the main surface of the semiconductor substrate and so as to leave the first insulating film within the trench;

depositing an intermediate insulating film over the main surface of the semiconductor substrate and the gate electrode;

etching back the intermediate insulating film overlying the main surface of the semiconductor substrate so as to entirely expose

the source region and the body contact region constituting the main surface of the semiconductor substrate; and

forming a source metal electrode over the main surface of the semiconductor substrate.

4. A method of manufacturing a vertical MOS transistor according to claim 2, wherein the first insulating film comprises a silicon nitride film.

5. A method of manufacturing a vertical MOS transistor according to claim 3, wherein the first insulating film comprises a silicon nitride film.

6. A method of manufacturing a vertical MOS transistor according to claim 3, wherein the thickness of the first insulating film falls within a range of 0.3 to 1.0 μm.

7. A method of manufacturing a vertical MOS transistor according to claim 6, wherein the first insulating film comprises a silicon nitride film.